EXTRACTING SYNCHRONOUS SECONDARY SIGNALS BY FUNCTIONAL ANALYSIS

ABSTRACT OF THE DISCLOSURE

Programmable devices include configurable logic hardware for implementing logic gates, registers for storing data, and secondary hardware for additional functions, such as loading and clearing. The secondary hardware can implement portions of the user design, thereby decreasing the number of gates to be implemented elsewhere. A set of possible alternative implementations of portions of the user design is identified by enumerating the inputs connected with a register. Logic diagrams are created for the set of inputs, and alternative implementations are identified from the logic diagrams by recognizing patterns similar to the secondary hardware functions. To determine an implementation that balances gate savings against routing costs, alternative implementations are grouped according to compatible inputs and ranked by the number of registers in each group. The implementation with the highest rank is selected, and selected registers are removed from other alternative implementations. The remaining alternative implementations are re-ranked for further selections.